IN THE DRAWINGS

The attached sheet of drawings includes a change to Fig. 10 This sheet, which includes Fig. 10 replaces the original sheet including Fig. 10

Attachment: Replacement Sheet

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following remarks is respectfully requested.

Claims 1-14 are presently active in this application.

In the outstanding Office Action the drawings were objected to, the abstract of the disclosure was objected to requiring correction, the disclosure was objected to as including informalities requiring correction, the title was objected to as being non-descriptive, Claims 1-4, 6 and 8-12 were rejected to under 35 USC §102(b) as being anticipated by Tanaka (US Pub. No. 2003/0042525), and Claims 5, 7, 13 and 14 were rejected under 35 USC §103(a) as being unpatentable over Tanaka.

In response to the several grounds for objection, the title, specification and abstract have been amended to correct each of the informalities identified in the outstanding Official Action. No new matter has been added.

However, in response to the requirement to submit a further cross-sectional view of the semiconductor device according to Claims 5 and 13, that ground for objection is traversed because the noted subject matter is believed to be adequately shown in Figures 7-10 as supported by the corresponding disclosure in the specification. Accordingly, the outstanding grounds for objection are believed to have been overcome, and it is respectfully requested that these grounds for objection be withdrawn.

Briefly recapitulating, pending Claim 1 recites:

> 1. A semiconductor device comprising:
> a drift layer of a first conductivity type;
> a collector layer of a second conductivity type located on the drift layer;
> a collector electrode located on the collector layer;
> a base layer of the second conductivity type located in a region isolated from the collector layer on the drift layer;
> a plurality of trenches formed at certain intervals to extend from the top surface of the base layer into the drift layer and thereby divide the base layer to main cell regions and dummy cell regions;

a first emitter layer of the first conductivity type selectively formed in the surface layer of the base layer in each main cell region to extend along adjacent one of the trenches;

gate electrodes formed in the trenches sandwiching each main cell region among said plurality of trenches via a gate insulating film;

an emitter electrode located over the base layer and the first emitter layer in each main cell region; and

a second emitter layer of the first conductivity type selectively formed so as to be scattered in the surface layer of the base layer in each dummy region and having a surface area smaller than that of the first emitter layer.

Claim 8 is similarly directed to a semiconductor device defined as follows:

8. A semiconductor device comprising:

a drift layer of a first conductivity type;

a collector layer of a second conductivity type located on the drift layer;

a collector electrode located on the collector layer;

a base layer of the second conductivity type located in a region isolated from the collector layer on the drift layer;

a plurality of trenches formed at certain intervals to extend from the top surface of the base layer into the drift layer and thereby divide the base layer to main cell regions and dummy cell regions;

a first emitter layer of the first conductivity type selectively formed in the surface layer of the base layer in each main cell region to extend along adjacent one of the trenches;

gate electrodes formed in the trenches sandwiching each main cell region among said plurality of trenches via a gate insulating film;

an emitter electrode located over the base layer and the first emitter layer in each main cell region; and

a second emitter layer selectively formed in the surface layer of the base layer in each dummy cell region,

wherein resistance value of a floating resistor as a resistance between the base layer of the dummy cell region and the emitter electrode is adjusted to be smaller than the resistance value causing rise of the gate-emitter voltage due to negative capacitance of the gate in a period to charge a gate charge between the gate and the collector by a voltage applied between the gate and the emitter when the device is turned on.

A common fundamental feature of Claims 1 and 8 is that a base layer of the second conductivity type is divided into main cell regions and dummy cell regions.

It is respectively submitted that Tanaka fails to disclose or obviate this common fundamental feature recited in pending Claims 1 and 8.

A further feature recited in Claim 8 is that the resistance value of a floating resistor as a resistance between the base layer of the dummy cell region and the emitter electrode is adjusted to be smaller than the resistance value causing rise of the gate-emitter voltage due to negative capacitance of the gate in a period to charge a gate charge between the gate and the collector by a voltage applied between the gate and the emitter when the device is turned on.

In contrast, Tanaka neither discloses nor suggests this feature of pending Claim 8. In view of these deficiencies identified in Tanaka, it is respectfully submitted that the outstanding grounds for rejection are traversed and that the pending claims patentably define over the cited art.

Consequently, in view of the present amendment to correct informalities, and in light of the above discussion distinguishing the claimed invention over the cited prior art, no further issues are believed to be outstanding, and the present application is believed to be in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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